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**Specifications**

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**Introduction**

In this design project, we will design, create, and test a BJT amplifier that adheres to the conditions stated in the lab specifications section noted above. The circuit and the calculations may have slightly different values, as the more exact values are calculated, however, they may not correspond to a proper E24 resistance value, so it will be changed to the closest possible resistance value.

**Circuit Under Test**

**Figure 1** below depicts the designed circuit which will be tested. The circuit consists of 3 stages: Stage 1: CC input with an input resistance of at least 40kΩ. Stage 2: CE with a high voltage gain, to ensure gain is not lost. Stage 3: CC output with a low output resistance. Capacitors in between stages are used to let AC signal pass, while denying DC signal. A switch was also implemented in order to be able to change between load and no-load amplifiers easily.

Diagram, schematic

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**Figure 1.** The amplifier circuit designed, split into its 3 stages.

Diagram

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**Figure 1(b).** Full image of 3-stage BJT amplifier circuit, without lines blocking any components.

**Experimental Results**

**DC Analysis**

|  |  |  |  |
| --- | --- | --- | --- |
| Circuit | Vs [mVp-p] | Vo [mVp-p] | Ve2 [V] |
| No load | 9.70 | 479 | 904 mV |
| Load | 9.70 | 437 | 903 mV |

**Table 1.** Measured voltage values of circuit design from **Figure 1.**

**Transient Response**

The circuit was set to transient operation mode and plotted the Vs and Vo responses of the circuit for both no load and loaded circuits. **Graph 1** will depict no load, while **Graph 2** will show the loaded graphs.

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**Graph 1.** No load Vo and Vs transient responses.

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**Graph 2.** Loaded circuit transient waveforms.

**Frequency Response**

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**Graph 3.** Frequency response of the output of the circuit.

We can see that from our graph, the maximum measured dB value was about 42 dB, but they are shown at -3dB. From our two cursors, we can see that the response is stable between around 19.9 Hz and 1MHz, which means that the proper specifications (20 Hz and 50kHz) are between these boundaries.

**Analysis**

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The no load Avo value is clearly within +/-10% of the target value of 50, meaning it is within the allowed limits. 90% of the no load value of 49.38 is 44.442. Our load Av is 45.05, and 45.05 > 44.44, meaning it is withing the specified requirements for the circuit.

**Evaluation**

**Choice of Configuration**

For the design, a three-stage circuit was used. The first was a CC input stage. This was chosen as it allowed us to have a high input resistance, as was required in the specifications. The second stage, the CE stage, was selected as it allowed us to have a high voltage gain, so that we do not lose as much voltage in the output. The final stage was a CC stage again. This is because the CC output stage allows us to have a low output resistance, which is required as we do not want to lose our voltage gain when a resistor load is attached.

**Transient Response**

There does not appear to be any clipping or other distortions in the **Graph 1 or 2.** This should indicate that the voltages are properly centered for each amplifier stage and the capacitor values were properly selected.

**Frequency Response**

In the circuit, the C3 capacitor was key, as it allowed us to have a lower operating minimum frequency. All other capacitors were then kept at a similar, high value. Because of this, the required specifications were met.

**Voltage Swing**

The value of Ve2 was around 1V, when rounded from the measurement. This ended up being the same value used in both load and no-load calculations as the value was very similar. Then, Vce,sat, which was estimated to be around 0.3V was added and this value was subtracted from Vcc. By doing this, we were sure that the specification requirements were met for both no-load and loaded circuits.

**Discrepancies/Distortions**

Most discrepancies or distortions were due to errors in rounding calculations. After rounding, the final values may have been slightly off, but the main source of error was most likely some of the resistor values. More exact values may have been calculated; however, most values did not correspond to a real E24 resistor value. This meant that a resistor value that was as close as possible to the calculated one had to be selected, and this may have altered the values, results, or graphs slightly, though it appears not enough to make the circuit not fall within specified requirements, meaning it was all fine still. While these values are still considered fine, it still did lead to discrepancies, such as a gain of about 49 instead of 50, even if it was acceptable. Also, the resistances and capacitances of the BJTs Also, the resistances and capacitances of the BJTs or the wire resistances were all ignored in the calculations, which may have slightly changed certain values.

**Conclusions**

In conclusion, this design seemed to work. I believe all requirements stated in the specifications were met, and it worked for both the no-load and loaded circuits. While there may have been slight discrepancies, they were stated in the discrepancies sub-section above. Calculations will be added into appendix, and the explanations have been stated above. The circuit was designed in a way that a real circuit such as this would be used; in a scenario in which we cannot change the value of the input voltage, as it would be supplied by something like the city of Toronto, and the load resistance has to be factored in, and must work for any load added such as a fridge being plugged in.

**Appendix**

**Calculations**

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Vt | Ic | R1 | R2 | Re1 | Re | Rin | Rout |
| 0.026 V | 0.7 mA | 43kΩ | 43kΩ | 7kΩ | 37.14Ω | 20.1kΩ | 243.54Ω |

**Table 2.** Stage 1; CC input stage values taken.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Vt | Ic | R3 | R4 | Re2a | Re2b | Re | Rin | Rout |
| 0.026 V | 0.7 mA | 45kΩ | 9235.2Ω | 118Ω | 0.805kΩ | 37.14Ω | 5.2kΩ | 8.1kΩ |

**Table 3.** Stage 2; CE amplifier values taken.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Vt | Ic | R5 | R6 | Re3 | Re | Rin | Rout |
| 0.026 V | 0.7 mA | 200kΩ | 200kΩ | 7.1kΩ | 37.14Ω | 95.4kΩ | 0.99kΩ |

**Table 4.** Stage 3; CC output stage values taken.

**Loading factors**

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**Miscellaneous**

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**Table 5.** List of E24 series resistors, but only under 220k resistors were used. All resistances were changed from calculated values to nearest E24 resistor value.